REMARKS

We acknowledge the Examiner's indication that claims 6 and 10 are allowable if amended to be in independent form and to include the features recited in any base and intervening claims. We have canceled claims 1 and 2 and have amended claims 3-10. With these amendments, claims 3-10 are currently pending with claims 3 and 7 being independent.

Prior Art Rejections

Independent Claim 1

The Examiner rejected claims 1 and 2 as being anticipated by Tsukihashi (U.S. 6,584,053). This rejection is moot in view of our having canceled claims 1 and 2.

Independent Claims 3 and 7

The Examiner rejected claims 3-5 and 7-9 as being anticipated by Tsukihashi. We submit that Tsukihashi does not disclose a controller including an address memory connected to the buffer memory, the address memory being configured to store a write-data-address of the data written to the recording medium and a read-data-address of the data read from the buffer memory when the writing of data to the recording medium is interrupted, wherein the write-data-address and the read-data-address each indicate a location of the data at which the interruption occurs, ... a retry determination circuit for determining whether an address of the written data, which is read from the recording medium, and the write-data-address, which is stored in the address memory, are the same ..., as recited in amended claims 3 and 7.

With respect to independent claim 3, we further submit that Tsukihashi does not disclose a controller including a second retry determination circuit for determining whether a first timing signal for reading the written data from the recording medium and a second timing signal for encoding the read data are the same ..., as recited in claim 3.

With respect to independent claim 7, we further submit that Tsukihashi does not disclose a synchronizing circuit determining whether a first timing signal for reading the written data

from the recording medium and a second timing signal for encoding the read data are the same ..., as recited in claim 7.

Among other advantages, the address memory of the invention stores a write-data-address, which indicates an interruption location of data written to the recording medium, and a read-data-address, which indicates an interruption location of data read from the buffer memory.

Tsukihashi discloses that the address data corresponding to the address of the last flame of the data which were output from the encoder 11 immediately before the interruption of recording are stored in the address memory 15a. That is, Tsukihashi merely discloses storing an address corresponding to data output from the encoder 11. Tsukihashi does not disclose storing two addresses indicating interruption locations of written data and read data.

Because claims 4-5 depend from independent claim 3 and claims 8-9 depend from independent claim 7, we further submit that these dependent claims are patentable for at least the same reasons that claims 3 and 7 are patentable.

The RCE fee ($790.00) and the Petition for Extension of Time Fee (two months) ($450.00) are being paid concurrently herewith on the Electronic Filing System (EFS) by way of Deposit Account authorization. Please apply any other charges or credits to Deposit Account No. 06 1050, referencing Attorney Docket Number 10449-030001.

Respectfully submitted,

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